REMARKS/ARGUMENTS

Applicant appreciates the Examiner's attention to this application. In view of the foregoing amendments and the following remarks, reconsideration of this application is respectfully requested.

Claims 1-2, 4-6, 12-13, 17-22, and 24-25 are now pending, with claims 1 and 12 being independent. This response cancels claims 3, 7-11, and 14-16 without prejudice; moves subject matter from claims 3 and 8 into claim 1; introduces further claim amendments; and adds new claims 24-25.

In particular, claim 1 has been amended to include subject matter from claims 3 and 8, along with further details pertaining to specific mechanisms used for communicating various specific signals within the electronic device.

For instance, claim 1 recites that the digital signal processor (DSP) comprises a "clock output pin" to provide a clock signal, a "digital data output pin" to provide the digital data output for conversion into analog data, and a "mode output pin" to provide a disable signal. In addition, claim 1 recites that the digital to analog converter (DAC) comprises corresponding inputs; e.g., a "digital data input pin" to receive the digital data for conversion, a "serial input pin" to receive the clock signal to enable reception of the disable signal, and a "mode input pin" to receive the disable signal. Furthermore, claim 1 recites that the DAC "reads the state of the disable signal at the rising edges of the clock signal." Claim 12 has been amended to recite similar features.

Claims 1-18 and 21-22 stand rejected under 35 U.S.C. § 103(a) as obvious over Mott et al. (6,170,060) in view of Seo et al. (5,063,597); Tran (5,734,729); and Nagata (6,114,981). Claims 19-20 stand rejected under 35 U.S.C. § 103(a) as obvious over Mott in view of Seo, Tran, Nagata, and Lipovski (6,675,002). Applicant respectfully traverses those rejections, at least to the extent that they might be applied to the current claims.

As indicated above, claim 1 involves a DAC with a mode input pin to receive a disable signal from a DSP. The Office Action asserts that Seo teaches (at col. 3, lines 32-38) a DAC that receives a mute signal from a DSP. Applicant respectfully traverses that assertion. The cited portion of Seo corresponds to Figure 3 of Seo. Although those portions of Seo involve a mute signal, that mute signal is not sent to a DAC. Instead, it is processed by a "counter 35," and it is used to control a "switch 39." Then, switch 39 sends a different signal – not the mute signal – to

the "D/A Converter." (Figure 3.) Specifically, according to Seo, the signal that switch 39 sends to the DAC is not a mute signal, but is instead either the raw "digital data" from "DSP 30" or digital data that was produced by DSP 30, and then processed through various other components (e.g., "multiplier 38") to provide a gradual shift to zero. (Col. 2, lines 62-68; col. 4, lines 40-49.)

Claim 1 also recites that the DAC comprises a serial input pin to receive the clock signal to enable reception of the disable signal. The Office Action asserts (in connection with old claim 3) that this feature is disclosed by Seo at column 3, lines 55-58. Applicant respectfully traverses that assertion. That portion of Seo says nothing about processing the disable signal. Instead, that portion of Seo refers to processing of the "digital data" of the DSP. According to Seo, this "digital data" is not the mute signal, but is instead the digital form of the actual content or payload; i.e., "a processed digital speech signal ... received from an analog-to-digital converter" (col. 2, lines 63-65).

Furthermore, Claim 1 explicitly recites that the DAC reads the state of the disable signal "at the rising edges of the clock signal." This response moves that subject matter from claim 8 into claim 1, with editing for clarification. The Office Action asserts (in connection with old claim 8) that this feature is taught by Seo at column 2, lines 62-66, and column 3, lines 14-18. Applicant respectfully traverses that assertion. Those portions of Seo do not indicate that the DAC reads the state of the disable signal at the rising edges of the clock signal. The first cited section indicates that the DSP outputs digital data, a word clock train, and a mute control signal, and the second cited section is poorly written, but it seems to say that the "counter 35" increments sequentially in response to the word clock train, when the mute control signal has a high state. However, neither of those sections says anything about reading the mute control signal at a rising edge of the clock signal.

Moreover, "counter 35" and the other components illustrated in Figure 3 of Seo are not even part of the DAC. Instead, the components of Figure 3, which are the subject of the text cited by the Office Action, belong to a "muting circuit" that actually includes the DSP (i.e., "DSP 30"). The muting signal from that muting circuit never gets to the DAC. Instead, the only signal that Figure 3 shows going to the "D/A Converter" is the output from "switch 39." As explained above, the signal that is put out by switch 39 is not the mute signal. By contrast, claim 1 refers specifically to the DAC, where claim 1 recites that "the digital to analog converter" reads the state of the disable signal at the rising edges of the clock signal.

For at least the foregoing reasons, the Office Action fails to establish a prima facie case of obviousness for claim 1.

The Office Action rejects claim 12 on the same bases as claim 1. However, as indicated above, claim 12 involves some or all of the features discussed above with regard to claim 1. Consequently, the Office Action also fails to establish a prima facie case of obviousness for claim 12.

The remaining claims depend ultimately from claim 1 or claim 12, and those dependent claims implicitly include the features of their parent claims. However, the rejections for the dependent claims, including the rejections for claims 19 and 20, do not supply the teachings necessary to establish a prima facie case of obviousness for the independent claims. Consequently, the Office Action also fails to establish a prima facie case of obviousness for any of the dependent claims. All claim rejections should therefore be withdrawn.

In addition, new claims 24 and 25 describe additional details for at least one embodiment of the invention. For instance, both of those claims refer to "mode data" from the digital signal processor that is read at the mode input pin of the digital to analog converter, "wherein the mode data comprises address bits, function bits, and a disable bit." Both of those claims also involve a DAC that reads the "disable bit within the mode data" as "the disable signal." The Office Action does not establish a prima facie case of obviousness for either of these new claims.

For all of the foregoing reasons, Applicant respectfully requests reconsideration of the present application. The Examiner is requested to contact Applicant's representative Indranil Chowdhury at (281) 772-9361 for further clarification and amendments to the claims for prompt prosecution and allowance of this application.

To the extent necessary, the Applicant petitions for an Extension of Time under 37 CFR 1.136. The Commissioner is authorized to charge any additional fees, including extension of time fees, and/or credit any overpayment to Deposit Account 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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